



ROSE MIU Testing

Vanderbilt University
Presented by Rebekah Austin



Acronyms

Acronym	Definition
ACS	Attitude Control System
ADC	Analog to Digital Converter
AUX	Auxiliary
C&DH	Command and Data Handling
CH	Channel
CLK	Clock
CURR	Current
DAC	Digital to Analog Converter
DC	Direct Current
Demux	De-multiplexor
DIGMUX	Digital Multiplexor
DIGTLM	Digital Telemetry
EDAC	Error Detection and Correction
FPGA	Field Programmable Gate Array
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LVDS	Low-voltage differential signaling

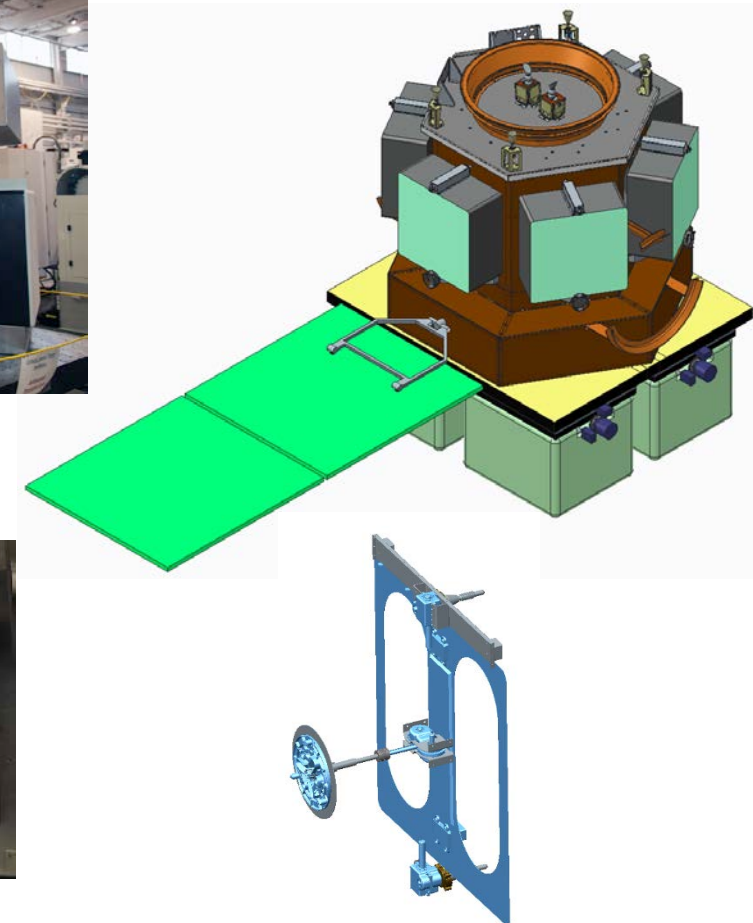
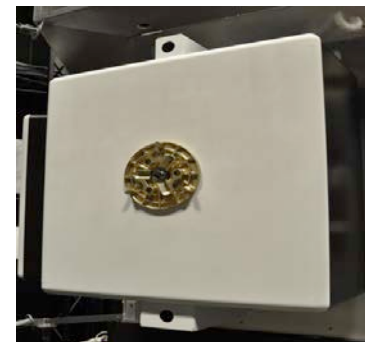
Acronym	Definition
MDM	Micro-D Metal Shell
MEM	Memory
MIU	Module Interface Unit
MUX	Multiplexor
NV MEM	Non-Volatile Memory
POL	Point of Load
POR	Power on Reset
ROSE	Reconfigurable Operational Spacecraft for Science and Exploration
RTN	Return
SCOMM	Serial Communication
SDRAM	Static Random Access Memory
SpaceFRAME	Space Flexible Reconfigurable and Modular Electronics
SW	Switch
THERM	Thermistor
TLM	Telemetry
UNSW	Un-switched



Overview of ROSE

- Low-cost spacecraft bus and instrument payload platform
- Serviceable spacecraft
- Reduce cost and schedule (after the first one)

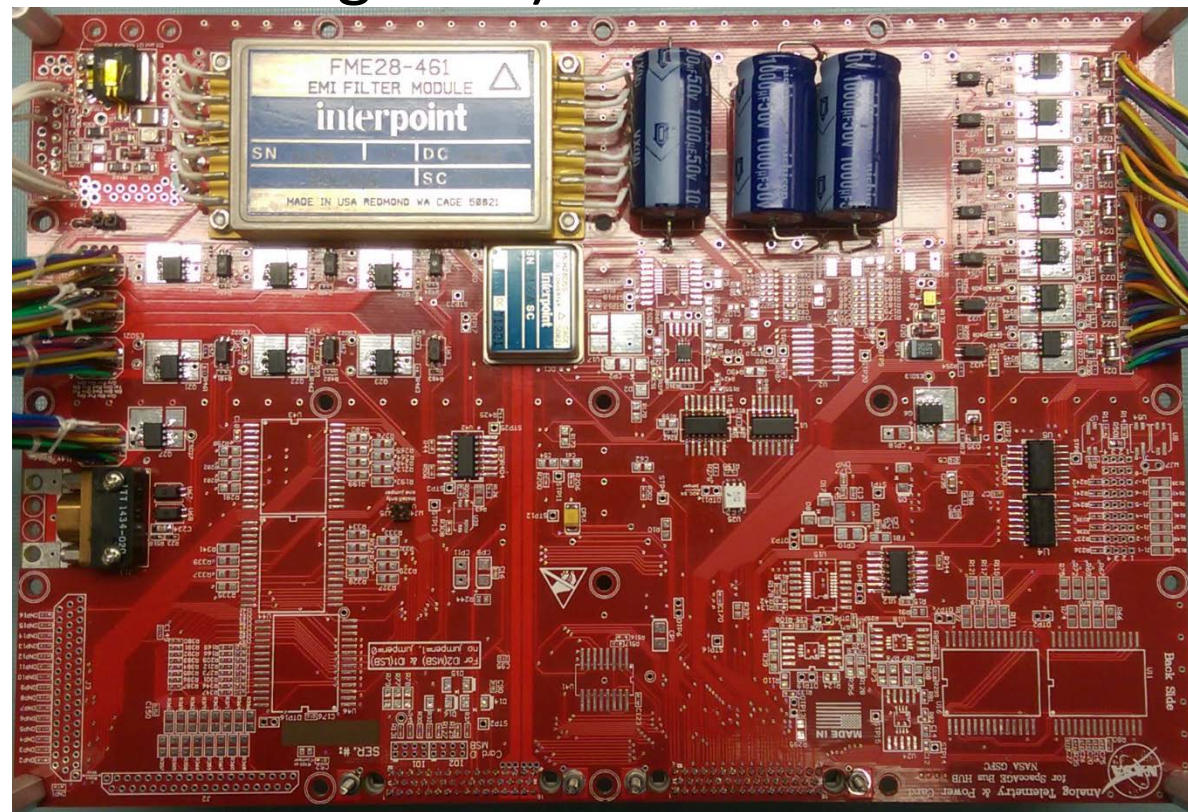
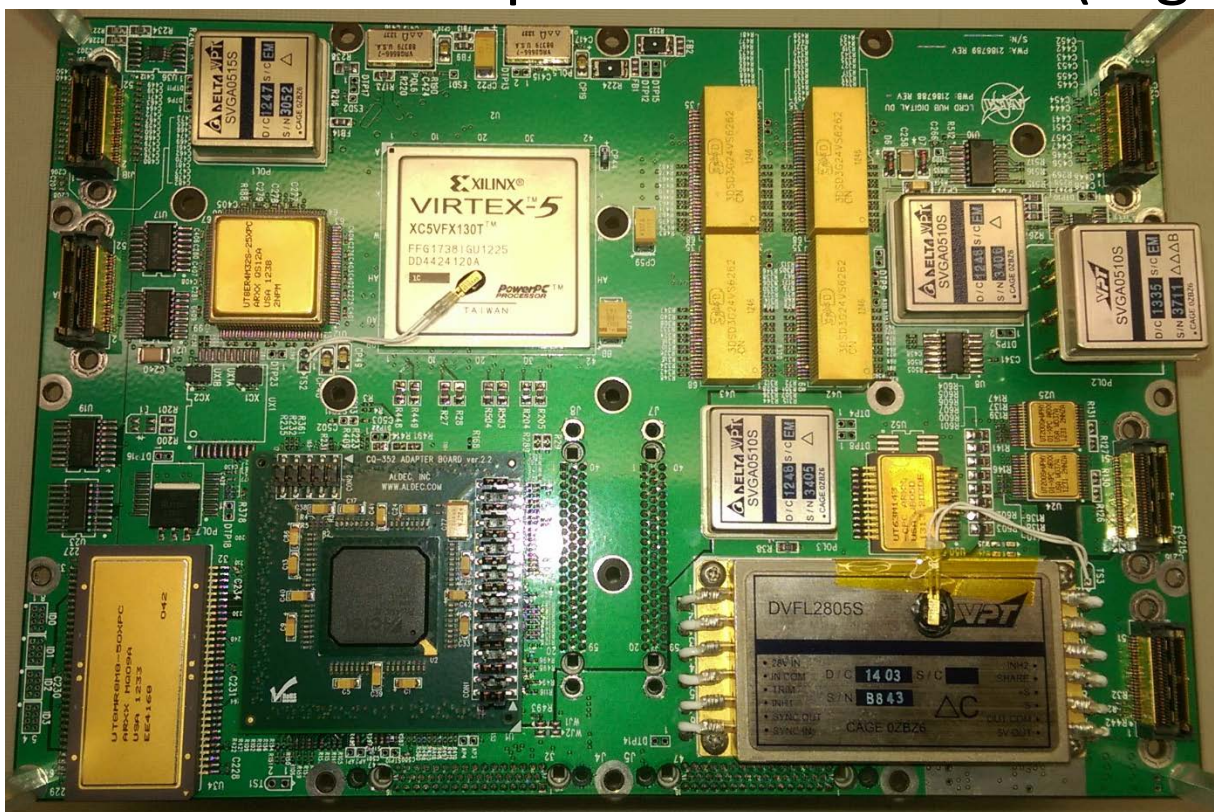
Module #	Description
1	Power
2	Reaction Wheel
3	Reaction Wheel
4	C&DH
5	ACS
6	Spare





Overview of MIU

- One in each module
- Baseline SpaceAGE Bus HUB (Digital and Analog Card)





HUB Functions

Digital Card

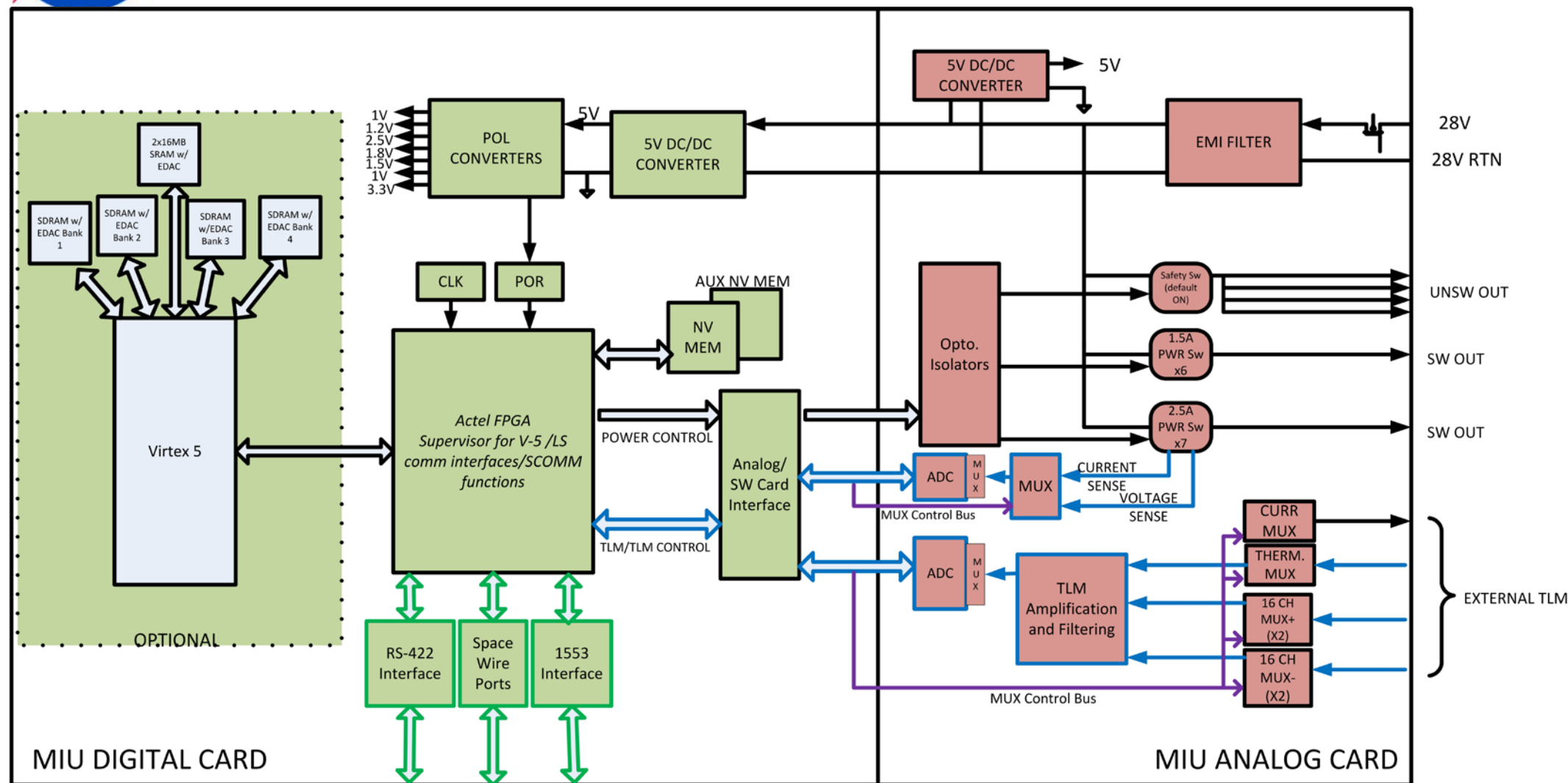
- Xilinx Virtex-5 with Microblaze processor
- Actel FPGA (Supervisory FPGA)
- 1553, SpaceWire, LVDS interfaces

Analog Card

- Seven 2.5A power switches (NODES)
- Six 2A power switches
- Two unswitched ports
- 16 differential telemetry channels
- 16 thermistor telemetry channels



Basic Functions of ROSE MIU



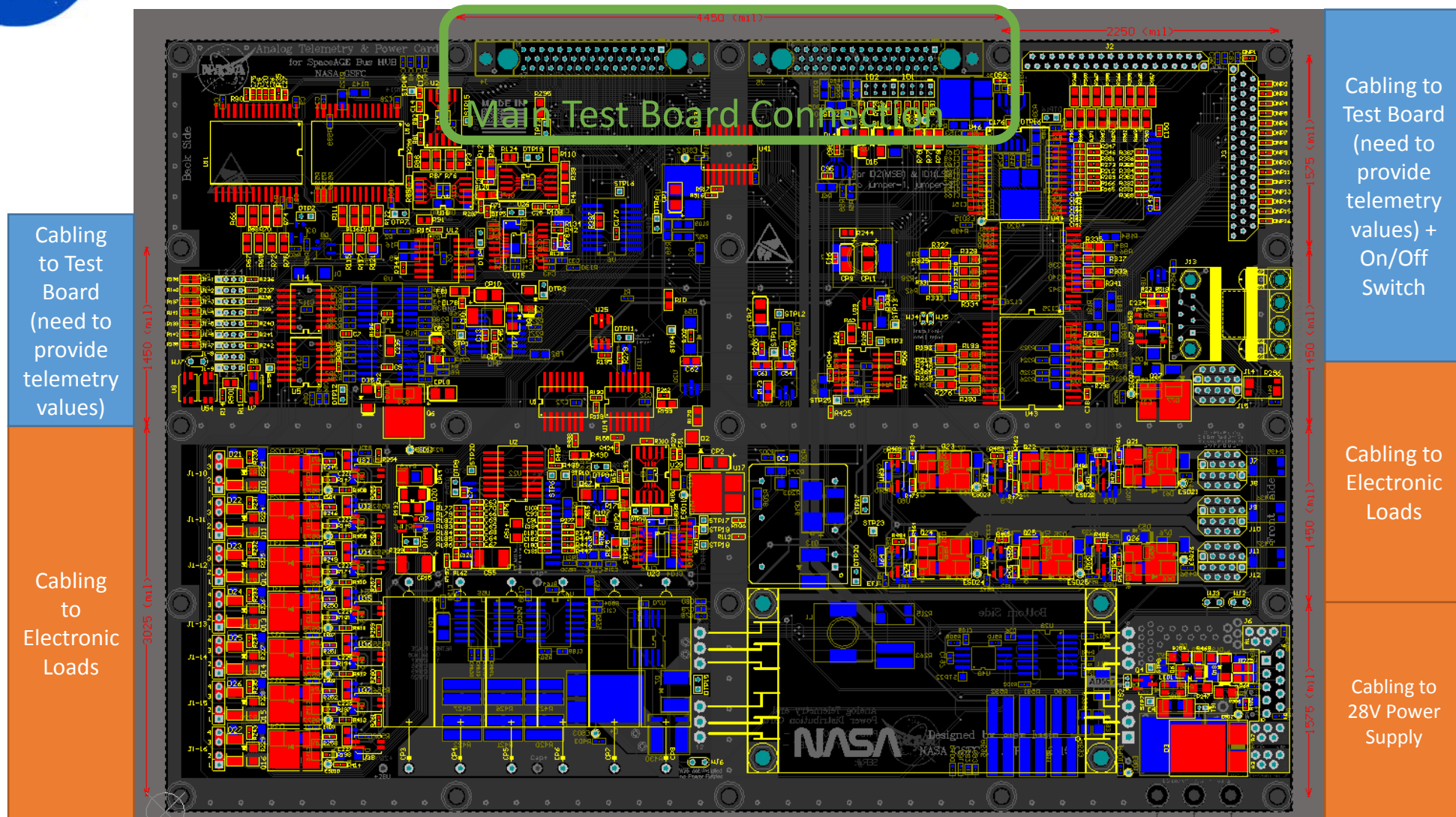


Analog Card Testing Overview

- Develop Test Board to mimic Digital Card
- Build switch only Analog Card, inspect, and test
- Build fully populated Analog Card, inspect, and test
- Create and implement test plan
- Build testing rack and software

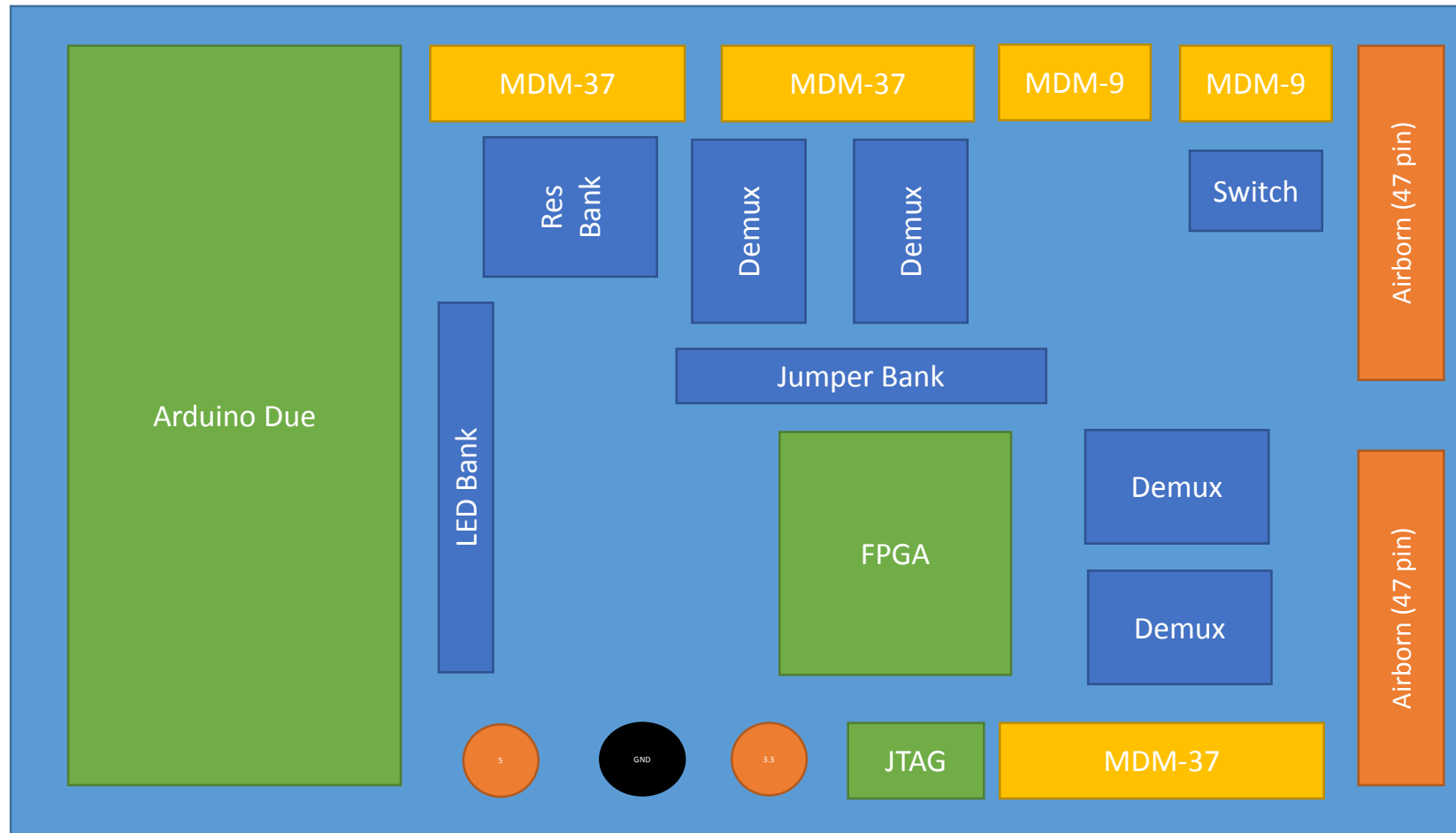


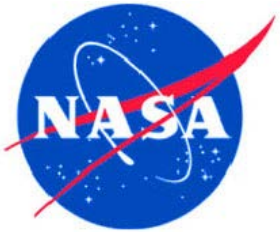
Analog Card Connections



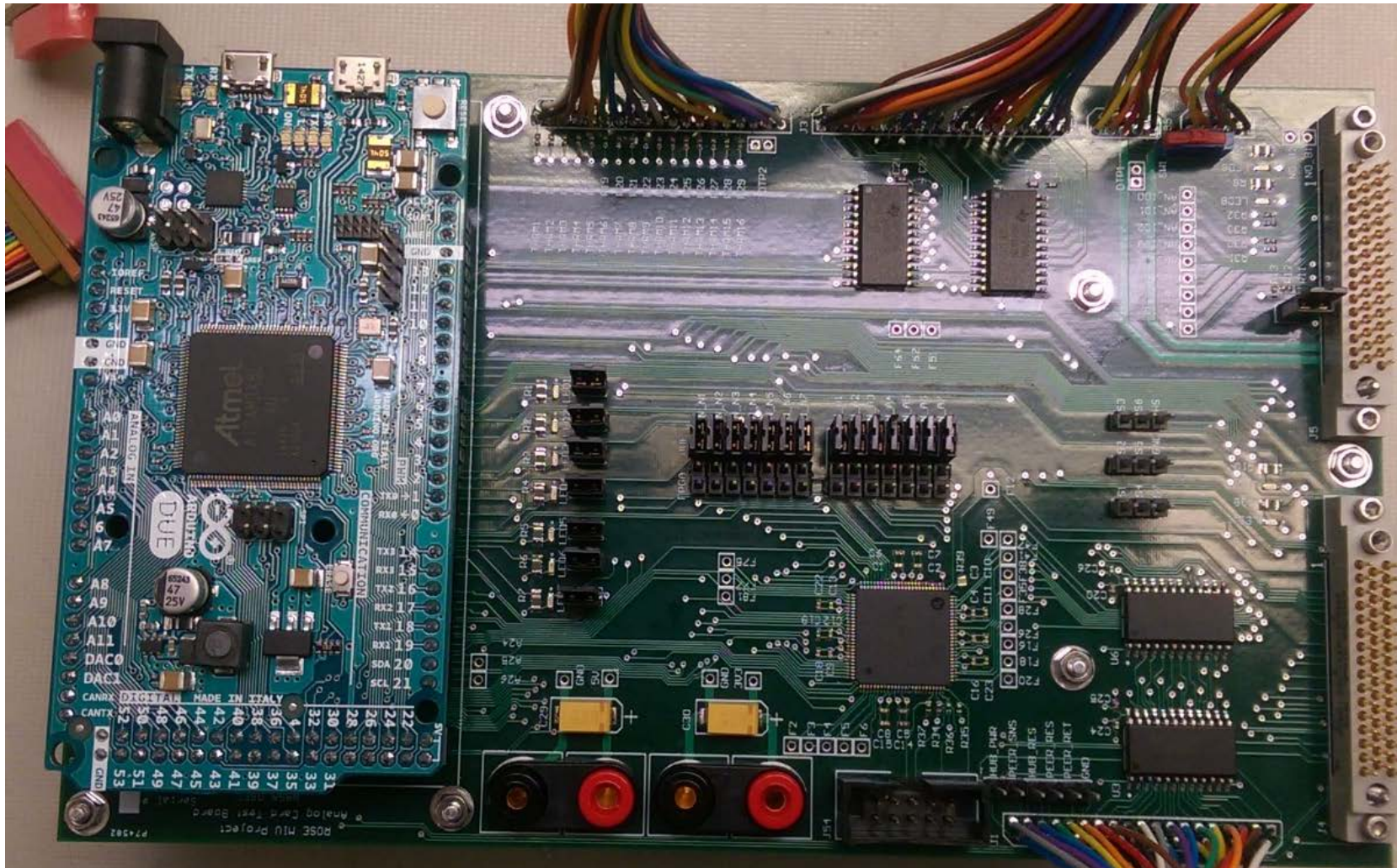


Test Board Block Diagram





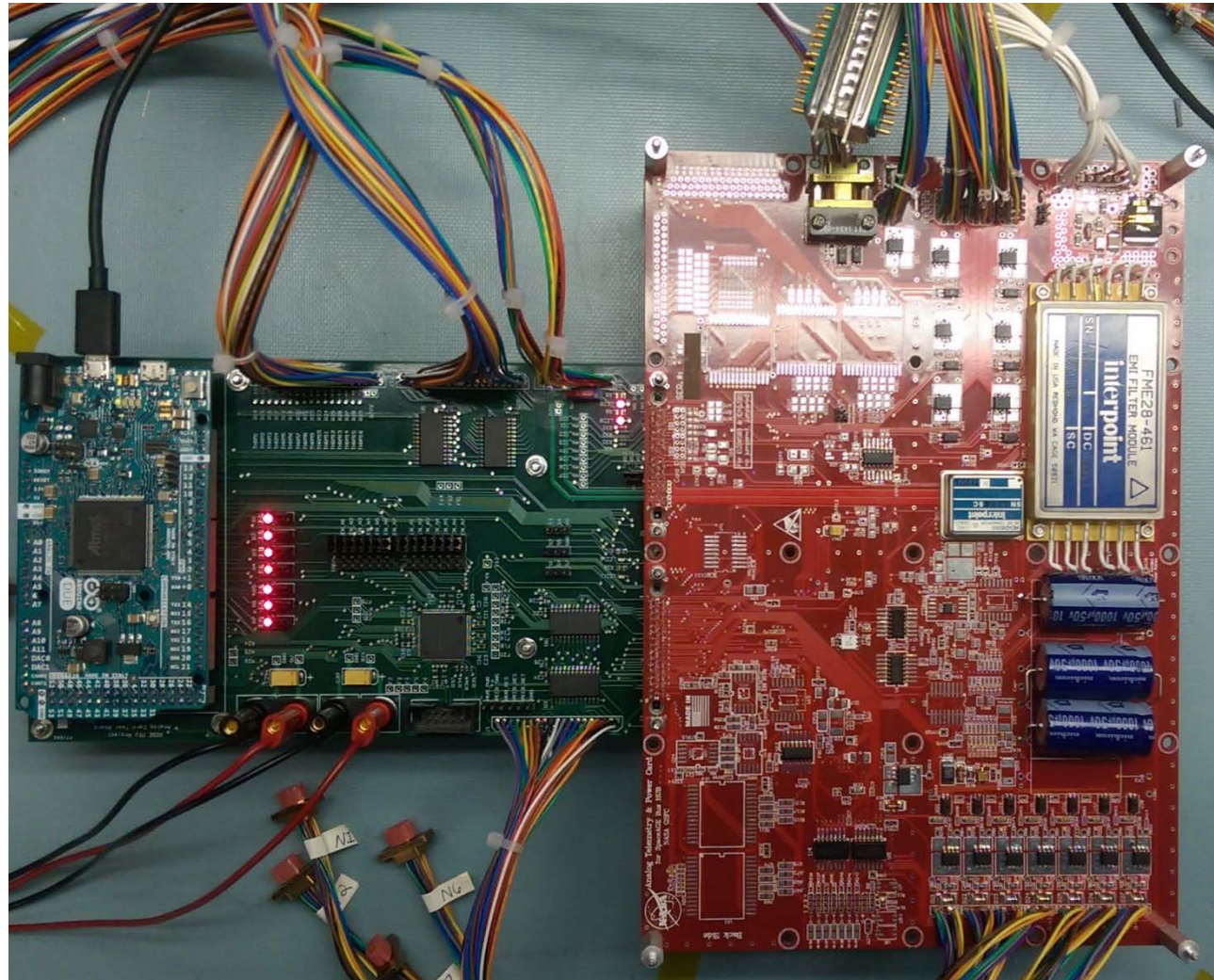
Test Board



To be presented by Rebekah A. Austin at Vanderbilt University, Nashville, Tennessee, September 10, 2015



Switch Only Board



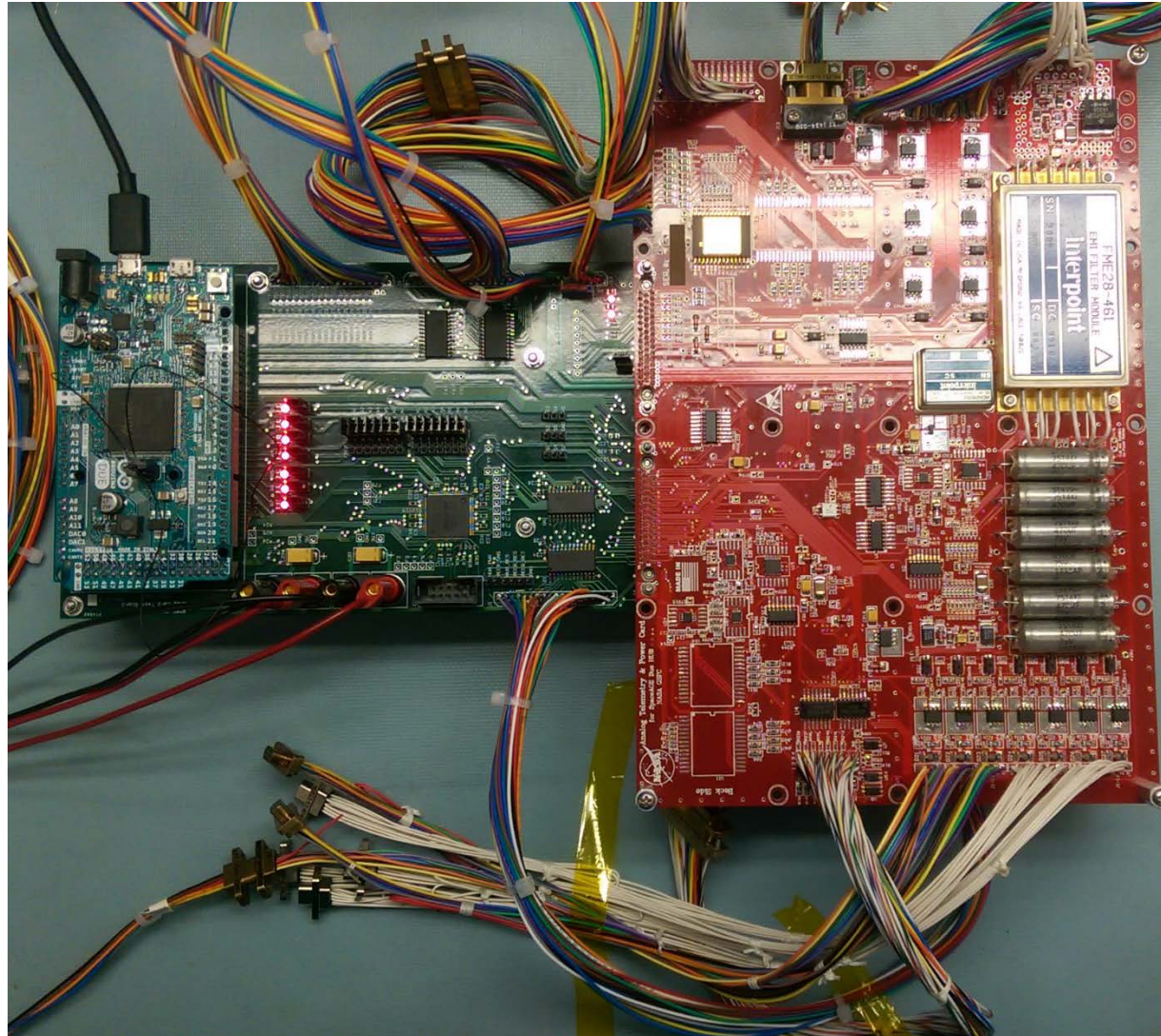


Challenges and Results

- Challenges
 - VOS628A-3T Optocoupler Issue
 - Grounding
 - Polarity on loads
- Results
 - All switches working individually as intended!



Fully Populated Board





Testing Priorities

1. Secondary ADC Interface
2. DAC Control
3. Power Fail Test/Reset
4. Turn off time
5. Primary ADC Interface
6. PEER HUB
7. DIGMUX
8. DIGTLM